REMARKS

The Applicant hereby traverses the rejections of record and requests reconsideration and withdrawal of such in view of the remarks herein. Claims 1, 15 and 23 have been amended to correct typographical errors. Claims 1-23 are pending in this application.

Objection to the Claims

Claims 14 and 22 are objected to as containing the trademark/trade name INTEL. Applicant respectfully disagrees. Claims 14 and 22 recite that "the plurality of processors are IA-64 processors." While the Examiner is correct that 'IA' is an abbreviation of 'Intel Architecture', Applicant asserts that IA-64 is not used a trademark or trade name, but rather as a identification of a particular computer architecture. A trademark or trade name is used to identify the source of the goods in question. IA-64 does not identify a source of goods, but merely compatibility with a particular computer architecture or standard. IA-64 processors may be manufactured by either Intel or Hewlett Packard, thus IA-64 does not identify a source, but rather a standard. IA-64 more properly categorized as a 'name used in trade' as defined under M.P.E.P. §608.01(v) which are permissible if their meaning is well known and satisfactorily defined in literature. The Examiner's citation to the wikipdia entry shows that the term is well known and satisfactorily defined in literature. Applicant, therefore, respectfully requests that the objection to claim 14 and 22 be withdrawn.

Rejection under 35 U.S.C. § 103 ()

Claims 1-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication No. 2003/0236972 to Harrington et al. (hereinafter, "Harrington") in view of U.S. Patent No. 6,742,139 to Forsman et al. (hereinafter, "Forsman"), U.S. Patent Publication No. 2002/0116469 to Okuyama (hereinafter, "Okuyama"), and U.S. Patent No. 6,820,207 to Dawkins et al. (hereinafter, "Dawkins").

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success.

Finally, the prior art cited must teach or suggest all the claim limitations. *see* M.P.E.P. § 2143. Without admitting that the second criteria is satisfied, the Applicant respectfully asserts that the Examiner's rejection fails to satisfy the first or third criteria.

Lack of All Claim Limitations.

Claim 1 requires executing, by one processor of the plurality of processors, a reset code from firmware, building a list of reset register addresses associated with the plurality of processors, sending an interrupt to the other processors of the plurality of processors, resetting the other processors by writing a reset code to their associated reset registers, and resetting the one processor by writing to its associated reset register. The combination put forth by the Examine does not describe these limitations.

The Examiner asserts that Harrington discloses executing, by one of the plurality of processors, a reset code from firmware. That Forsman discloses "a multiprocessor system wherein the service processor itself or a host will set a bit within the service processor's status/control register (reset register) to cause an interrupt thus causing a reset it failure is detected" And that Dawkins discloses a multiprocessor system wherein the service processor in cooperation with NVRAM creates (builds) objects (table stored in NVRAM which is inclusive of addresses) that consists of profiles used to configure and manage processors within the logical partition, that Dawkins further discloses sending an interrupt to the other processors of the plurality of processors, and further discloses resetting (activating) the other processors by activating the system reset signals in all of the processors.

Applicant respectfully disagrees with the Examiner's characterization of Dawkins. The Examiner has stated that Dawkins shows a service processor in cooperation with NVRAM which creates (builds) objects (table stored in NVRAM which is inclusive of addresses) that consists of profiles used to configure and manage processors within the logical partition, citing column 10, lines 16-18 and column 5, line 63 through column 6, line 6. Column 10, lines 16-18 states "Next, the service processor updates NVRAM processor table set target address to 0x100 for all processors of the partition (step 802)." The section continues in lines 18-22: "This address points to a location to which all processors will look to after being reset. Then, the service processor activates the system reset signal to all processors of the partition (step 804) with the process terminating thereafter." Column 5, line 63 through column 6, line 6 states that management of the logical partitions is achieved

through terminals using the service process and NVRAM, and that NVRAM contains objects such as profiles used to configure and manage the logical partitions. Nowhere in the sections cited by the Examiner does Dawkins disclose building a list of reset register addresses associated with the plurality of processors. Dawkins merely states that the NVRAM includes profiles used to configure and manage the logical partitions, and that the service processor can set a target address in the NVRAM that the slave processor can look to after reset. These two statements do not equate to building a list of reset register addresses associated with the plurality of processors as required by claim 1.

Claims 2-14 depend from claim 1 and therefore inherit all the limitations thereof. Claims 2-14, therefore, are allowable for at least the reasons set forth above with respect to claim 1.

Lack of Motivation

The mere fact that references can be combined does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *see In re Mills*, 916 F.2d 680 (Fed. Cir. 1990); M.P.E.P. § 2143. Applicant respectfully submits that neither Forsman, nor Harrington provides motivation for the combination, as the Examiner suggests.

The Examiner's stated motivation for combining Harrington with Forsman is "to include having an interrupt sent to the service processor to reset the processor by setting a bit within it's status/control register (reset register) as taught by Forsman such that the one processor that reset all of the other partition processors is interrupted and reset by writing to its associated reset register", citing column 1, lines 31-38. The citation by the Examiner has nothing to do with resetting all the processors in a logical partition including the processor executing the reset code. The citation by the Examiner states that the invention of Forsman relates to reestablishing communication between a service processor and a host after the service process has stopped functioning properly where heartbeat signals from the service processor indicate whether the service processor is functioning properly.. Forsman at column 1, lines 31-38.

Applicant would point out that all of Harrington and Forsman are systems utilizing service processors to manage logical partitions having multiple processors. See Figures 2 and

3 of Harrington and Figure 1 of Forsman. Yet neither of the references describe resetting the other processors by writing a reset code to their associated reset registers, and resetting the one processor by writing to its associated reset register. Harrington describes resetting partition processors but not the service processor and Forsman describes resetting the service processor but not the partition processors. Neither provides any indication of motivation to perform the task described by the other. Applicant respectfully asserts, therefore, that neither reference provides motivation, nor the mechanism for making the combination cited by the Examiner.

Applicant would respectfully assert that the suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on the Applicant's disclosure. M.P.E.P. 2142, citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). For the reasons set forth above Applicant respectfully asserts that there is no motivation to combine Harrington and Forsman. Applicant, therefore, respectfully requests that the rejections based on the combination of Harrington and Forsman be withdrawn.

Rejection under 35 U.S.C. § 103 (Harrington in view of Dawkins)

Claims 15-16 and 21-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Harrington in view of Dawkins.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *see* M.P.E.P. § 2143. Without admitting that the first or second criteria are satisfied, the Applicant respectfully asserts that the Examiner's rejection fails to satisfy the third criteria.

Lack of All Claim Limitations.

Claim 15 requires firmware comprising reset code that resets a portion of the partition, wherein one processor of the plurality of processors executes the reset code, and

random access memory that is not affected by the reset code, that stores a list of addresses associated with the portion.

The Examiner states that Harrington does not disclose random access memory that is not affected by the reset code that stores a list of addresses associated with the portion, and relies upon Dawkins as describing this limitation citing column 5, line 63 through column 6, line 6. As described with reference to claim 1, the cited portion of Dawkins merely states that the NVRAM contains objects such as profiles used to configure and manage logical partitions. No reference is made in Dawkins that the NVRAM stores a list of addresses associated with the portion as required by claim 15. As the combination of Harrington and Dawkins does not describe each and every limitation of claim 15, Applicant respectfully submits that claim 15 is allowable over the rejection of record.

Claims 16 and 21-22 depend from claim 15 and therefore inherit all the limitations thereof. Claims 16 and 21-22, therefore, are allowable for at least the reasons set forth above with respect to claim 15.

Rejection under 35 U.S.C. § 103 (Dawkins in view of Forsman)

Claim 23 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Dawkins in view of Forsman.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *see* M.P.E.P. § 2143. Without admitting that the first or second criteria are satisfied, the Applicant respectfully asserts that the Examiner's rejection fails to satisfy the third criteria.

Lack of All Claim Limitations.

Claim 23 requires means for building a list of reset register addresses associated with the plurality of processors, means for placing each processor of the plurality of processors

into a known state, and means for resetting the plurality of processors by writing a reset code into their associated reset registers.

The Examiner relies upon Dawkins as describing building a list of reset register addresses associated with the plurality of processors. For the reasons set forth with respect to claim 1 and 15, the Applicant respectfully disagrees with the Examiner's characterization of Dawkins. Dawkins only describes that the NVRAM holds a profile used to configure and manage the logical partition. Dawkins does not describe building a list of reset register addresses associated with the plurality of processors as required by claim 23.

Further, the Examiner states that Dawkins does not disclose writing a reset code into the plurality of processors associated reset registers, and relies upon Forsman as describing this limitation citing column 3, lines 51-55 and column 4, lines 31-38). The cited potions of Forsman only describe the service processor of Forman resetting by setting a bit in the control potion of the status/control register. Forman does not describe means for resetting a plurality of processors by writing a reset code into their associated reset registers as required by claim 23. As the combination of Dawkins and Forsman does not describe each and every limitation of claim 23, Applicant respectfully submits that claim 23 is allowable over the rejection of record.

Rejection under 35 U.S.C. § 103 (Harrington and Dawkins in view of Forsman)

Claims 17-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Harrington and Dawkins as applied to claim 15 further in view of Forsman.

Claims 17-20 depend from claim 15 and therefore inherit all the limitations thereof. Claims 17-20, therefore, are allowable for at least the reasons set forth above with respect to claim 15.

Conclusion

In view of the above remarks, the Applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge Deposit Account No. 08-2025, under Order No. 200205355-1 from which the undersigned is authorized to draw.

Dated: September 1, 2006

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV568253338US, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: September 1, 2006

Signature: _____
Jan Cleveland